REMARKS

Claims 1, 5, 8, 12, 26, 30, 33, and 37 are currently pending in the application.

Claims 2 through 4, 6, 7, 9, 10, 11, 13 through 16, 27 through 29, 31, 32, 34 through 36, 38, and 39 have been canceled.

This amendment is in response to the Office Action of September 16, 2002.

Applicants note the acceptance of the corrected drawings filed on July 8, 2002, with appreciation.

Claims 8 through 11 and 33 through 36 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 1 through 4 and 26 through 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (United States Patent 5,313,096) in view of Kohno et al. (United States Patent 5,293,068).

Claims 5, 6, 30, and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (United States Patent 5,384,689) in view of Kohno et al. (United States Patent 5,293,068).

Claims 8 through 11 and 33 through 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (United States Patent 5,099,309) in view of Kohno et al. (United States Patent 5,293,068).

Claims 12, 14 through 16, 36, and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (United States Patent 5,099,309) in view of Kohno et al. (United States Patent 5,293,068) and Shen (United States Patent 5,384,689).

Claims 7 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen (United States Patent 5,384,689) and Kohno et al. (United States Patent 5,293,068) as applied to claims 5 and 30 above, and further in view of Degani et al. (United States Patent 5,473,512).

Claims 13 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (United States Patent 5,099,309), Kohno et al. (United States Patent 5,293,068),

and Shen (United States Patent 5,384,689) as applied to claims 12 and 37 above, and further in view of Degani et al. (United States Patent 5,473,512).

Applicants have amended the claimed invention for the presently claimed invention to comply with the provisions of 35 U.S.C. § 112, first paragraph, and to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112, second paragraph.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over any combination of the cited prior art for any rejection under the provisions of 35 U.S.C. § 103.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicant submits that any combination of all the cited prior art in the application does not and cannot under any circumstances establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of amended claims 1, 5, 8, 12, 26, 30, 33, and 37. Applicant submits that any combination of the cited prior art cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed because any combination of the Eide reference and the Kohno et al. reference, at the very least, cannot be combined , there is no suggestion for any combination thereof, if combined, does not teach or suggest all the claim limitations of the presently claimed invention, and any combination thereof would be a hindsight reconstruction of the presently claimed invention based solely upon Applicant's disclosure by picking and choosing elements of the claimed

invention among the elements of the cited prior art.. For instance, the Eide reference does not teach or suggest the presently claimed elements of the claimed invention calling for " said semiconductor die is attached to second substrate having an upper surface without recesses therein . . . , providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over-chip configuration on said surface, providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the second substrate, applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto, attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate, connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate, filling at least a portion of the via in the substrate with a sealant, connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, and the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins" and "for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon . . . , providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface, providing a first substrate having a die side surface, a second

attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate, filling a potion of the via in the substrate with a sealant, applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto, attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said substrate, connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate; and attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins". In contrast to the presently claimed invention, the Eide reference does not teach or suggest any method of attaching a semiconductor die in any fashion. Additionally, Applicant submits that the Kohno et al. reference fails to teach or suggest the claim limitations of the present invention calling for "A method of electrically connecting a semiconductor die to a first substrate when said semiconductor die is attached to second substrate having an upper surface without recesses therein . . . ,providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over-chip configuration on said surface, providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the second substrate, applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto, attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate, connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate, and filling at least a

portion of the via in the substrate with a sealant, connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins" and "A method of attaching a semiconductor die to a first substrate for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon , . . . ,providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface, providing a first substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate, filling a potion of the via in the substrate with a sealant, applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto, attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said substrate, connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate, and attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins". Applicant further submits that any combination of the Eide reference in view of the Kohno et al. reference fails to teach or suggest the claim limitations of the present invention of amended claims 1 and 26 calling for "" said semiconductor die is attached to second substrate having an upper surface without recesses therein . . . , providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface

having a plurality of bond pads extending in a leads-over-chip configuration on said surface, providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the second substrate, applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto, attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate, connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate, filling at least a portion of the via in the substrate with a sealant, connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, and the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins" and "for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon . . . , providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface, providing a <u>first</u> substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate, filling a potion of the via in the substrate with a sealant, applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto, attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of

said substrate, connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate; and attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins", "A method of electrically connecting a semiconductor die to a first substrate when said semiconductor die is attached to second substrate having an upper surface without recesses therein . . . ,providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over-chip configuration on said surface, providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the second substrate, applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto, attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate, connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate, and filling at least a portion of the via in the substrate with a sealant, connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins" and "A method of attaching a semiconductor die to a first substrate for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon, .

. . ,providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface, providing a first substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate, filling a potion of the via in the substrate with a sealant, applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto, attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said substrate, connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate, and attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins".

Applicant submits that not only does the cited prior art fail to teach or suggest such claim limitations but, further, the cited prior art fails to contain any suggestion whatsoever for any combination thereof. The proposed combination of the cited prior art is nothing more than a hindsight reconstruction of Applicant's claimed invention by attempting to pick and choose among the features of the cited prior art in a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. No motivation for any combination of the cited prior art has been clearly set forth whatsoever. Additionally, the cited prior art clearly teaches away from any combination thereof whatsoever. The Eide reference stacks a plurality of substrates on a substrate 10 wherein the Kohno et al. reference merely attaches a semiconductor die to a substrate. Neither cited prior art reference uses solder balls or pins to connect a substrate to another substrate or master board.

Therefore, presently amended claims 1 and 26 are clearly allowable over any combination of the cited prior art because the cited prior art cannot and does not establish a *prima facie* case of obviousness regarding the presently claimed invention under 35 U.S.C. § 103.

Similarly regarding presently amended claims 5 and 30, Applicant submits that the cited prior art does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention because the cited prior art, at the least, does not teach or suggest all the claim limitations, the cited prior art teaches away from any combination thereof, and any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure.

Applicant submits that any combination of the cited prior art fails to teach or suggest the limitations of the presently claimed invention calling for "A method of electrically connecting a semiconductor die to a master board . . . , providing a semiconductor die having a plurality of bond pads thereon, providing a master board having a plurality of circuit traces on an upper surface thereof, said upper surface having no recesses therein, providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board, providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board, attaching said semiconductor die to a portion of the die side surface of the board, connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board, and connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board using one of a plurality of solder balls and a plurality of pins, said board being located above the upper surface of said master board" and "A method of attaching a semiconductor die to a master board . . . , providing a semiconductor die having at least one bond pad thereon, providing a master board having at least one circuit trace on an upper surface thereof, said upper surface free of any recess for the receipt of a semiconductor die therein, providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second

attachment surface, at least one circuit, and at least one bond pad located on the second attachment surface of the board, providing at least one electrical connector for connecting the at least one bond pad located on the second attachment surface of the board to the at least one circuit trace of the master board, attaching said semiconductor die to a portion of the die side surface of the board, connecting said at least one bond pad of said semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through the at least one via extending through then board, and connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board using at least one of at least one solder ball and at least one pin as a connector".

Applicant submits that not only does the cited prior art fail to teach or suggest such claim limitations but, further, the cited prior art fails to contain any suggestion whatsoever for any combination thereof. The proposed combination of the cited prior art is nothing more than a hindsight reconstruction of Applicant's claimed invention by attempting to pick and choose among the features of the cited prior art in a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. No motivation for any combination of the cited prior art has been clearly set forth whatsoever. Additionally, the cited prior art clearly teaches away from any combination thereof whatsoever. The Shen is directed to attaching a semiconductor die in a recess in a substrate or in a spacer stacked on a substrate wherein the Kohno et al. reference merely attaches a semiconductor die to a substrate. Neither cited prior art reference uses solder balls or pins to connect a substrate to another substrate or master board.

Therefore, presently amended claims 5 and 30 are clearly allowable over any combination of the cited prior art because the cited prior art cannot and does not establish a *prima facie* case of obviousness regarding the presently claimed invention under 35 U.S.C. § 103.

Considering presently amended claims 8 and 33, Applicant submits that any combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because the cited prior art, at the least, does not teach or suggest all the claim limitations, the

cited prior art teaches away from any combination thereof, and any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure.

Applicant submits that any combination of the cited prior art fails to teach or suggest the claim limitations of the present invention calling for "A method of electrically connecting at least two semiconductor die to a first substrate for connection to circuit traces on the upper surface of a second substrate, said upper surface having no recesses therein for a semiconductor die . . . ,providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface, providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate, applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto, attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate, filling at least a portion of each via in the substrate with a sealant; and connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface having bond pads for the at least two semiconductor die electrical connection with said traces on said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins, said first substrate for locating above the upper surface of said second substrate" and "A method of attaching at least two semiconductor die to a first substrate for connection to a second substrate having at least one circuit on an upper surface thereof, said upper surface without any

recess for the receipt of at least one semiconductor die therein . . . , providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having at least one bond pad extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface, providing a first substrate having a die side surface, a second attachment surface, at least two vias extending through the first substrate from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the first substrate, applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto, attaching the surface having at least one bond pad thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the first substrate having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the first substrate, connecting said at least one of each of the semiconductor die to said at least two bond pads of said first substrate using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface having bond pads for the at least two semiconductor die for electrical connection with an electrically conductive circuit connected to said pads, filling at least a portion of each via in the first substrate with a sealant, and connecting said first substrate to the upper surface of the second substrate using one of at least one solder ball and at least one pin ".

Applicant submits that not only does the cited prior art fail to teach or suggest such claim limitations but, further, the cited prior art fails to contain any suggestion whatsoever for any combination thereof. The proposed combination of the cited prior art is nothing more than a hindsight reconstruction of Applicant's claimed invention by attempting to pick and choose among the features of the cited prior art in a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. No motivation for any combination of the cited prior art has been clearly set forth whatsoever. Additionally, the cited prior art clearly teaches away

from any combination thereof whatsoever. The Kryzaniwsky reference is directed to attaching a semiconductor die in a recess in a substrate wherein the Kohno et al. reference merely attaches a semiconductor die to a substrate. Neither cited prior art reference uses solder balls or pins to connect a substrate to another substrate or master board.

Therefore, presently amended claims 8 and 33 are clearly allowable over any combination of the cited prior art because the cited prior art cannot and does not establish a *prima facie* case of obviousness regarding the presently claimed invention under 35 U.S.C. § 103.

Further when considering presently amended claims 12 and 37, Applicant submits that any combination of the cited prior art fails to establish a establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because the cited prior art, at the least, does not teach or suggest all the claim limitations, the cited prior art teaches away from any combination thereof, and any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure.

Applicant submits that any combination of the cited prior art fails to teach or suggest the claim limitations of the invention calling for "A method of electrically connecting a plurality of semiconductor die to a master board . . . , providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface, providing a master board having a plurality of circuit traces located on an upper surface thereof, said upper surface being free of any recess for the location of a semiconductor die therein, providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board, providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board, attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board, connecting

said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through the board, and connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board using one of a plurality of solder balls and a plurality of pins, said board being located above the upper surface of said master board" and "A method of attaching a plurality of semiconductor die to a master board . . . , providing a plurality of semiconductor die, each semiconductor die being one of a semiconductor die having at least one bond pad extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface, providing a master board having a plurality of circuit traces on the upper surface thereof, the upper surface being free of semiconductor die recesses therein , providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board, providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board, attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board, connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through then board, and connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on the upper surface of said master board using one of solder balls and pins as connectors".

Applicant submits that not only does the cited prior art fail to teach or suggest such claim limitations but, further, the cited prior art fails to contain any suggestion whatsoever for any combination thereof. The proposed combination of the cited prior art is nothing more than a hindsight reconstruction of Applicant's claimed invention by attempting to pick and

choose among the features of the cited prior art in a hindsight reconstruction of the claimed invention based solely upon Applicant's disclosure. No motivation for any combination of the cited prior art has been clearly set forth whatsoever. Additionally, the cited prior art clearly teaches away from any combination thereof whatsoever. The Kryzaniwsky reference is directed to attaching a semiconductor die in a recess in a substrate wherein the Kohno et al. reference merely attaches a semiconductor die to a substrate and wherein the Shen reference is directed to attaching a semiconductor die in a recess in a substrate or in a spacer stacked on a substrate. None of the cited prior art references uses solder balls or pins to connect a substrate to another substrate or master board.

Therefore, presently amended claims 12 and 37 are clearly allowable over any combination of the cited prior art because the cited prior art cannot and does not establish a *prima facie* case of obviousness regarding the presently claimed invention under 35 U.S.C. § 103.

In summary, for the reasons set forth herein, Applicants request the allowance of claims 1, 5, 8, 12, 26, 30, 33, and 37 and the case passed for issue.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Three Times Amended) A method of electrically connecting a semiconductor die to a first substrate when said semiconductor die is attached to second substrate having an upper surface without recesses therein, comprising:

providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over-chip configuration on said surface;

providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the second substrate;

applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto;

attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate; [and]

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said substrate;

filling at least a portion of the via in the substrate with a sealant;

connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below

said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins.

5. (Amended) A method of electrically connecting a semiconductor die to a master board, comprising:

providing a semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces on an upper surface thereof, said upper surface having no recesses therein [thereon];

providing a board having a die side surface, a second attachment surface, [at least one via] a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the at least one via extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board using one of a plurality of solder balls and a plurality of pins, said board being located above the upper surface of said master board.

8. (Four Times Amended) A method of electrically connecting at least two semiconductor die to a first substrate for connection to circuit traces on the upper surface of a

second substrate, said upper surface having no recesses therein for a semiconductor die, comprising:

providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the substrate;

applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto;

attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate;[and]

filling at least a portion of each via in the substrate with a sealant; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface having [retaining unused] bond pads for the at least two semiconductor die [to have the ability for] electrical connection with [an electrically conductive device] said traces on said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins, said first substrate for locating above the upper surface of said second substrate [connected to said pads].

12. (Three Times Amended) A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die being a semiconductor die having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface;

providing a master board having a plurality of circuit traces <u>located on an upper surface thereof, said upper surface being free of any recess for the location of a semiconductor die therein</u> [thereon];

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through the board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board <u>using one of a plurality of solder balls and a plurality of pins, said board being located above the upper surface of said master board</u>.

26. (Three Times Amended) A method of attaching a semiconductor die to a first substrate for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon , comprising:

providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface;

providing a first substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate;

filling a potion of the via in the substrate with a sealant

applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto;

attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said substrate; [and]

connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate; and

attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins.

30. (Twice Amended) A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace on an upper surface thereof, said upper surface free of any recess for the receipt of a semiconductor die therein [thereon];

providing a board having a die side surface, a second attachment surface, a plurality of vias [at least one via] extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the second attachment surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the second attachment surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through the at least one via extending through then board; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board using at least one of at least one solder ball and at least one pin as a connector.

33. (Four Times Amended) A method of attaching at least two semiconductor die to a first substrate for connection to a second substrate having at least one circuit on an upper surface thereof, said upper surface without any recess for the receipt of at least one semiconductor die therein , comprising:

providing at least two semiconductor die, each semiconductor die being one of a semiconductor die having a surface having at least one bond pad extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface;

providing a first substrate having a die side surface, a second attachment surface, at least two vias extending through the first substrate from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the first substrate;

applying an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto;

attaching the surface having at least one bond pad thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the first substrate having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the first substrate; [and]

connecting said at least one of each of the semiconductor die to said at least two bond pads of said first substrate using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the substrate; the second attachment surface having [retaining unused] bond pads for the at least two semiconductor die for [to have the ability for] electrical connection with an electrically conductive circuit [device] connected to said pads;

filling at least a portion of each via in the first substrate with a sealant; and

connecting said first substrate to the upper surface of the second substrate using one of at least one solder ball and at least one pin .

37. (Twice Amended) A method of attaching a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die being one of a semiconductor die having at least one bond pad extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over configuration on said surface;

providing a master board having a plurality of circuit traces on the upper surface thereof, the upper surface being free of semiconductor die recesses therein [thereon];

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a

plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the plurality of vias extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on the upper surface of said master board using one of solder balls and pins as connectors.